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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,405	01/15/2004	Jun Takinosawa	MORI0006	4937

24203 7590 08/09/2006

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EXAMINER

MARTINEZ, DAVID E

ART UNIT PAPER NUMBER

2181

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/757,405	Applicant(s) TAKINOSAWA ET AL.	
	Examiner David E. Martinez	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-6 and 8-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz Fleming

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

8/7/2006

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3/16/04.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11, 12-16, 17-19, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

1. With regards to claims 11 and 20, line 4 of claim 11, and line 13 of claim 20 refer to the term "arbitrary write data". It is not clear what the term means. Write data can only be definite in a digital system and thus 'arbitrary write data' is indefinite.

Claim 12 recites the limitation "the Secure Digital Input Output host device" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim. Furthermore, in line 13 of claim 12, the term "via the one" renders the claim indefinite. It is understood from line 9 that there exists at least 2 application interfaces, however, when using "via the one" makes it unclear as to which one of the application interfaces is being referred to.

Claim 17 recites the limitation "the Secure Digital Input Output host device" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim. Furthermore, in line 16 of claim 12, the term "via the one" renders the claim indefinite. It is understood from line 8 that there exists at least 2 application interfaces, however, when using "via the one" makes it unclear as to which one of the application interfaces is being referred to.

With further regards to claim 20, in lines 1-2 and in line 4, it recites the term "a Secure Digital Input Output host device" which renders the claim indefinite since it's not clear if the term refers to only one instance of a Secure Digital Input Output host device, or if it's referring to two distinct instances of such a device. Also, in line 2 it calls for "a Secure Digital Input Output

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application” and in line 4, it also calls for “a Secure Digital Input Output application”. Are those supposed to be the same instance of a Secure Digital Input Output application or are they separate and distinct from each other?

Due to claims 13-16 and 18-19 being dependent from claims 12 and 17 respectively, they suffer from the same deficiencies as their parent claims and thus are rejected under the same rationale.

Due to the vagueness and a lack of clear definiteness in the claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. US 2001/0006902 A1 to Ito. In view of US Patent No. 6,748,482 to Fackenthal.

With regards to claim 20, Ito teaches a method of transmitting write data from a Secure Digital Input Output host device to a Secure Digital Input Output application, the method comprising the steps of:

(a) connecting a Secure Digital Input Output application [fig 2 element 10] with a Secure Digital Input Output host device [fig 2 element 10 operably connected to a host], wherein the Secure Digital Input Output application comprises a Secure Digital Input Output controller [fig 2

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element 21] having a Secure Digital interface [fig 2 element 21f] and an application interface [fig 2 element 21e];

(b) receiving a write command from the Secure Digital Input Output host device via the Secure Digital interface and interpreting the command [paragraphs 38, 82-83 when receiving a command, the host must send its personal identification which is sent to the SD memory card];

(c) generating a command response signal using the Secure Digital interface and sending the command response signal to the Secure Digital Input Output host device [paragraphs 38, 82-83 – the SD memory card sends a response if it allows itself to be used by the host];

(d) after the Secure Digital Input Output host device receives the command response signal, transmitting data from the host device to the Secure Digital Input Output controller via the Secure Digital interface [fig 2 element 10 being an SD memory card can receive write data after authenticating the host], wherein the transmitted data includes at least a register read/write address [done in a write or read operation], a selected type of operation [done in a write or read operation], a quantity of data [done in a write or read operation], and arbitrary write data [done in a write or read operation] in a digital system [the SD card is being used in conjunction of a host computer];

(e) decoding the transmitted data using a microcontroller unit of the Secure Digital Input Output controller [see paragraphs 6, 38 and 44].

2. Ito teaches all of the above limitations but is silent as to step (f): accessing non-contiguous register addresses of registers in the Secure Digital Input Output application via the application interface by using the microcontroller unit so data sent from the Secure Digital Input Output host device is written into the registers of the Secure Digital Input Output application. However, Fackenthal teaches it is common for an application interface to access data in flash

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memory from contiguous and non-contiguous registers for the benefit archiving data into available memory registers even if they are scattered, for being able to retrieve data at a later time [column 1 lines 24-42].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Ito and Fackenthal to access non-contiguous register addresses of registers in the Secure Digital Input Output application via the application interface by using the microcontroller unit so data sent from the Secure Digital Input Output host device is written into the registers of the Secure Digital Input Output application for the benefit archiving data into available memory registers even if they are scattered, for being able to retrieve data at a later time.

Allowable Subject Matter

Claim 1-2, 4-10, 21 allowed over the prior art of record.

Note claim 11 which ultimately depends from claim 1, requires further clarification in order to overcome the 35 U.S.C. 112, 2nd paragraph rejection.

Claims 12 and 17 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record, alone or in combination do not teach or fairly suggest the following limitations which are found in claims 1, 12, and 17:

An SDIO controller including application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface and a UART interface; and a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary memory and the application interfaces.

Response to Arguments

Applicant's arguments filed 5/30/06 directed to claim 20 have been fully considered but they are not persuasive. Applicant's arguments directed to claim 20 fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. During the last office action dated 1/30/06, the Examiner rejected claim 20 as being a combination of limitations found in claims 1, 11 and 12, thus meeting the initial burden of establishing a prima facie case. It is the Applicant the one that made no attempt to argue how the cited references fail to anticipate claim 20 and only alleges that it does so without any analysis.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

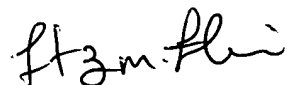
Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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